EAST Browser - L4: (1) precharge ad.. | US 5831924 | Tag: S | Doc: 1/1 | "Full" 1/45 (Total images 45)

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TITL... ynchronous
semi... ice having a
plurality of banks
distributed in a plurality of memory
arrays

---------- KWIC ----------

Detailed Description Text - DETX (41):

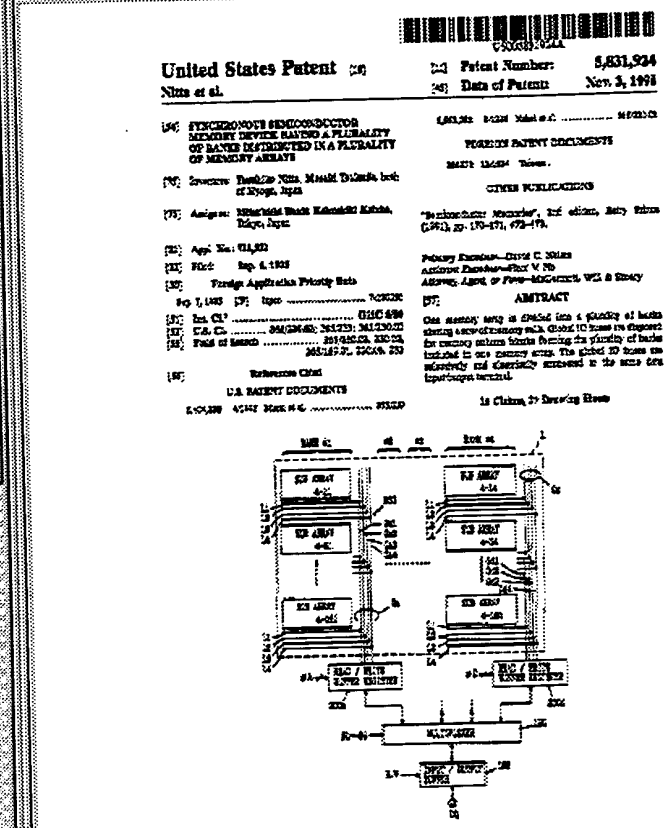
In the operation timing chart illustrated in FIG. 5, banks #1 and #2 attain a precharge state by activating signal /RAS and a write enable signal WE (not shown) to a low level at the rise of clock signal CLK. As a result, a precharge command is given and the designated bank is precharged.

Detailed Description Text - DETX (112):

While the local IO bus and the global IO bus are each formed by a complementary signal line pair in the embodiments described above, such 1-bit bus can be formed by one signal line.

Details Text Image HTML KWIC

L4: (1) precharge ad.. | US 5831924 | Tag: S | Doc: 1/1 | "Full" 1/45 (Total i...



United States Patent [19]
Nitta et al.

[11] Patent Number: 5,831,924
[45] Date of Patent: Nov. 3, 1998

SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE HAVING A PLURALITY OF BANKS DISTRIBUTED IN A PLURALITY OF MEMORY ARRAYS

[57] ABSTRACT

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L21: (13) 20 and memory | US 5319753 A | Tag: S | Doc: 1/13 | For...

(7) In many systems, it is useful for an interrupting device to pass more information than just an interrupt vector to an interrupted processor. Such additional information flowing from a higher-level or supervisory processor to a lower-level or slave processor is commonly called "Commands," while information in the other direction is commonly called "Status." Information that doesn't fit these categories is simply called "Messages."

(8) Accordingly, one object of the present invention is to provide an interrupt mechanism that facilitates the passing of interrupt vectors and associated supplementary command /status/message information (hereinafter referred to as "items of interrupt information") generated by one device to another device.

(9) Another object of the present invention is to provide an interrupt mechanism that facilitates not only the passing of interrupt information between devices, but also the queuing and subsequent reading of such queued interrupt information by the device being interrupted.

(10) Still other objects of the present invention are to provide a queued interrupt mechanism that is flexible with respect to the type and amount of

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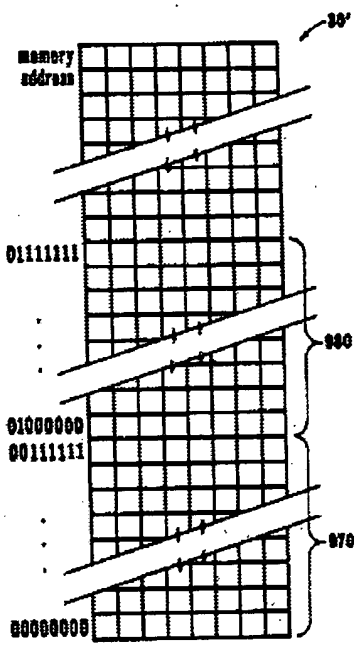

FIG. 4.

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(71) The DAM request pulse arriving at the central microprocessor 14 initiates a response there. The central processor 14 completes those operations which it had started before arrival of the DMA request and had not yet completed. Thus, when a DMA request arrives, the central microprocessor is not turned off immediately; some time passes before its disconnection (all output buffers of the central processor occupy a high-ohm resistance value). During this time span, while the central processor 14 is still in communication with the main memory 15, it must be ensured that the preprocessor 13 remains disconnected from access to the main memory 15.

(72) This is done in simplest manner by the clock delay member 268. This delay member is a frequency demultiplier which reduces the clock frequency at which the preprocessor 13 is clocked in the normal state to a much lower value compared with the normal value. In the present embodiment, the normal value of the clock frequency is about 4 MHZ, representing a pulse interval of the clock pulses of 0.25 .mu.s. When the clock delay member 268 is activated by the DMA pulse, it reduces the clock frequency to a value of about 0.33 MHZ. The interval between clock pulses is then about 3 .mu.s.

(73) The normal value of the clock frequency is given by a clock pulse generator 269, which furnishes the timing both for the central processor 14 and for the preprocessor 13. The pulses of the clock pulse generator 269 pass via line 270 to the frequency demultiplier 268. As long as the latter is switched to normal operation, the clock pulses of line 270 are passed undelayed via line 271 to the preprocessor 13 as operating clock pulses. But if a DMA request pulse is applied at the frequency demultiplier, the cycle described above occurs, in which the clock frequency of the pulses of line 270 is reduced in the manner described. Then only clock pulses of reduced frequency reach the preprocessor 13 via line 271. Preprocessor 13 is thereby delayed in its cycle; it is not yet ready for communication despite the DMA request having been issued. This situation changes the moment an acknowledgement signal is given by the central processor 14, whereby the central processor confirms that its own communication with the main memory 15 is terminated.

(74) In FIG. 16, this acknowledgement signal appears as DMA-enable signal in the output line 272 of the central processor. Thence it is applied via a line branch 273 on the one hand to the clock delay member 268; on the other head, it

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(13) Also shown in FIG. 2, the MMID comprises a plurality of data and control interfaces to the QMUD, the BED, the ICIC and the external memory array. The main functional units of the MMID include 1) the memory input/output (MIO) buffers, which buffer the signals used to access the memory array, 2) the DP operation registers, which can be programmed via the DC component for operational control of the DP component, 3) the data path unit (DPU), which transfers and converts the data from the QMUD buffers to the selected memory locations and vice versa via unidirectional read and write data busses, 4) the ICIC, which includes the ICIC buffers, the system-side interface to the DP component (SYSIDP) and the memory -side interface to the DP component (MEMIDP) for buffering data and commands received from the MCL of the DC component and converting the commands into data transfer control signals, and 5) the datapath state machines (DPSMs), which provide the control for all other data path blocks based on the current command from the MCL via the ICIC.

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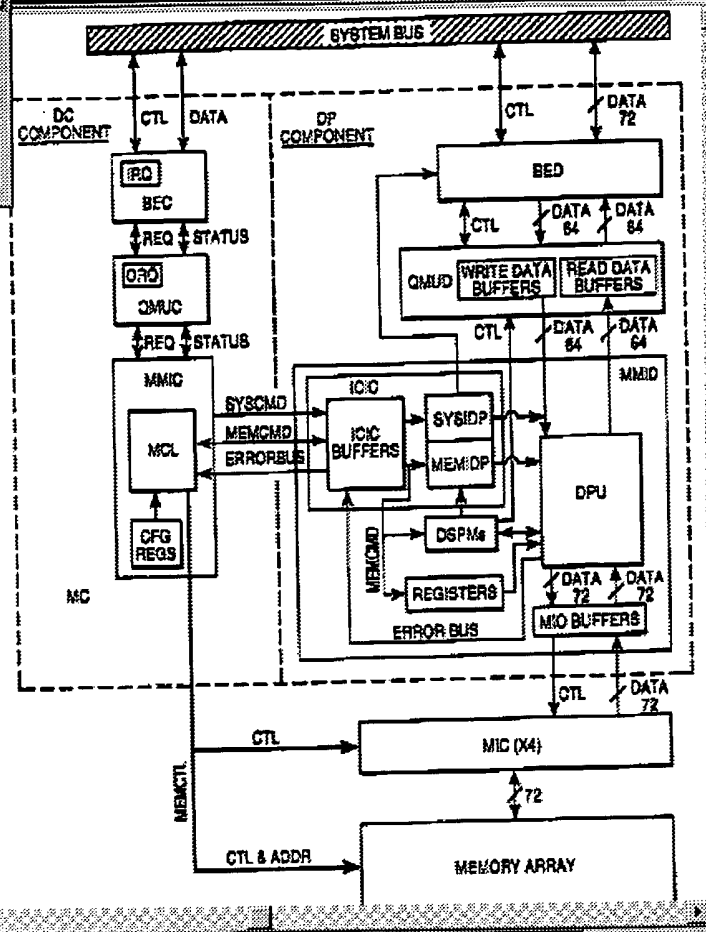

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DATE-ISSUED: May 5, 1998

INVENTOR-INFORMATION:
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APPL-NO:    08/ 581034

DATE FILED:  December 29, 1995

INT-CL: [ 06]  G11C008/00

US-CL-ISSUED: 365/230.03;365/230.06
;365/189.02 ;365/230.02

US-CL-CURRENT: 365/230.03 ; 365/189.02 ;
365/230.02 ; 365/230.06
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Boise, both of Id.

Technology, Inc., Boise, Id.

1998

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365/230.03; 365/230.06; 365/189.02; 365/230.02

arch 365/230.03, 238.5, 365/230.02, 236, 189.02, 230.06

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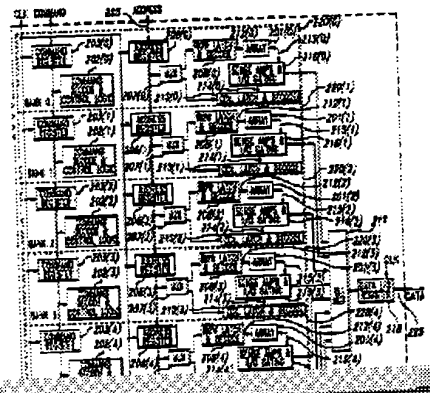
990	Fromm et al.	711/169
991	Wise et al.	365/230.03
993	Matsuda et al.	365/230.03
996	Russa	365/230.03

GN PATENT DOCUMENTS

989	European Pat. Off. .
988	Germany .
994	WIPO .

dynamic random access memory device (SDRAM). a memory array and associated circuitry are divided into multiple internally defined circuit banks. Commands and addresses applied to the memory device affect all internal banks identically, but on a time-staggered basis. In an eight bank embodiment, activation of a selected row is first initiated in Bank0 by registration of an ACTIVE command and a coincident row address. One system clock cycle later, activation of the selected row is initiated in Bank1, and so on until activation of the selected row is initiated in Bank7 seven clock cycles after the initial registration of the command. A READ or WRITE command and coincident column address can be applied after the activation time limit has been met for the selected row in Bank0. The READ or WRITE command then affects successive banks in the above-described time staggered manner. Similarly, a PRECHARGE command can be applied when the read latency or write recovery time limit has been met for Bank0, and this command is executed in a time staggered manner in the successive banks. In a four bank embodiment, command registration and execution is staggered every two successive system clock cycles.

24 Claims, 19 Drawing Sheets



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(8) With the invention, data can be written to multiple columns at the same time. This is accomplished by overriding the specified column(s)` sense amplifiers during the write command with FBdata(127:0). The column(s) are driven back to the corresponding internal storage cells. The data write is further qualified by the Byte Write Enable BWEN(15:0) signal. Each bit in BWEN enables one byte of data to be written. There are 16 bytes of data in the 128-bit FBdata(127:0) signal. Consequently, there are 16 bits of BWEN associated with each write command. BWEN can change every clock thus giving the controller the power to convert a read-modify-write cycle into a write cycle only. This is very different from a conventional SGRAM write mask since SGRAM write masks comes from registers, it cannot change on the fly with data . The Precharge command invalidates the sense amplifier's latched data and forces it to an unknown state. If a read or write command applies to an array that is not activated (i.e., precharged), an error message is generated. Various

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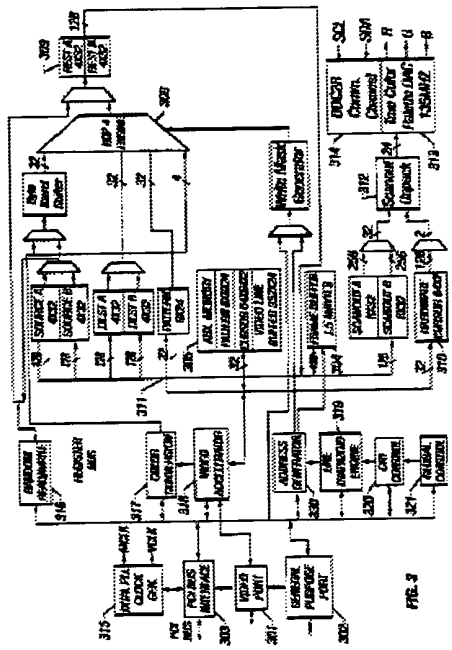

FIG. 3

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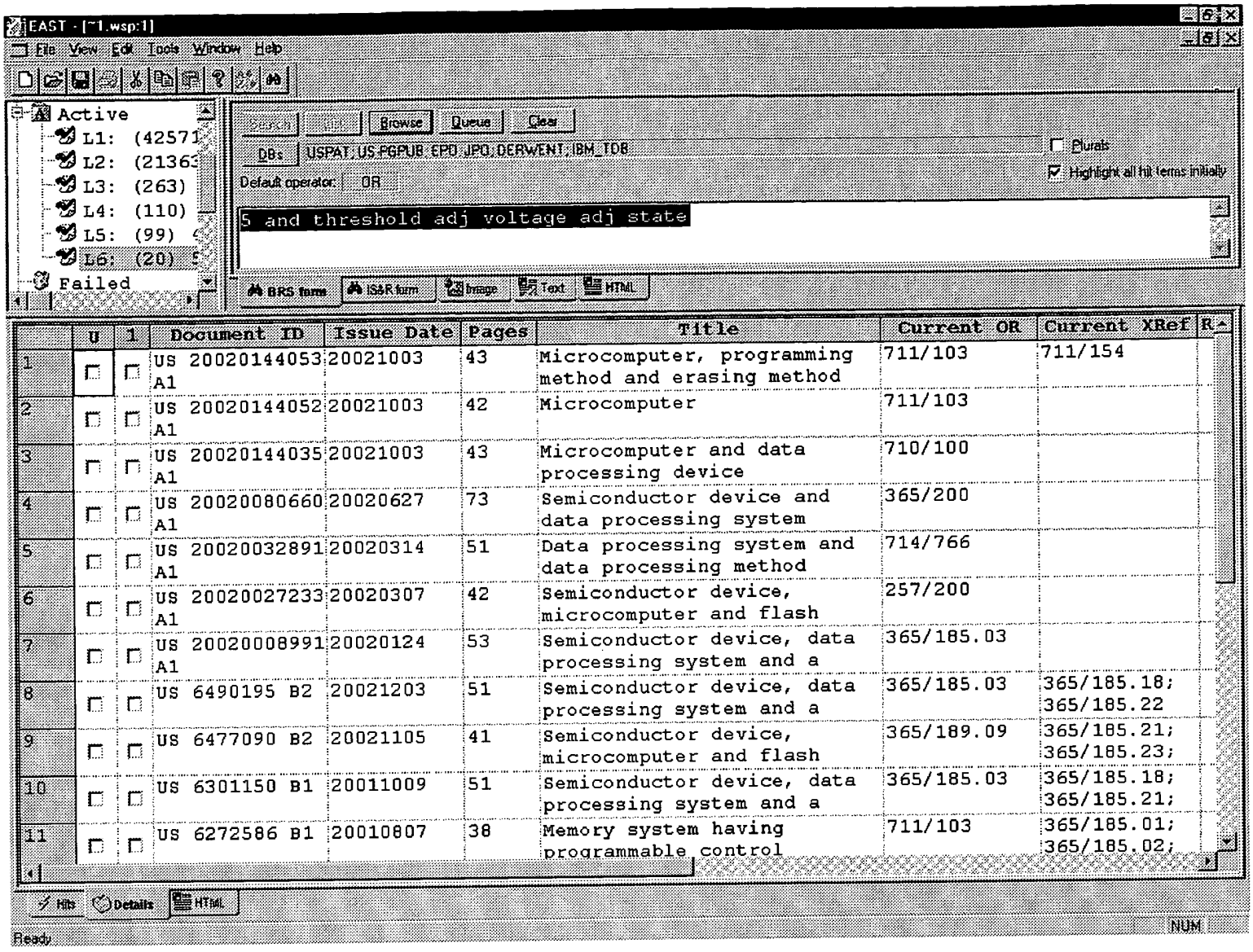
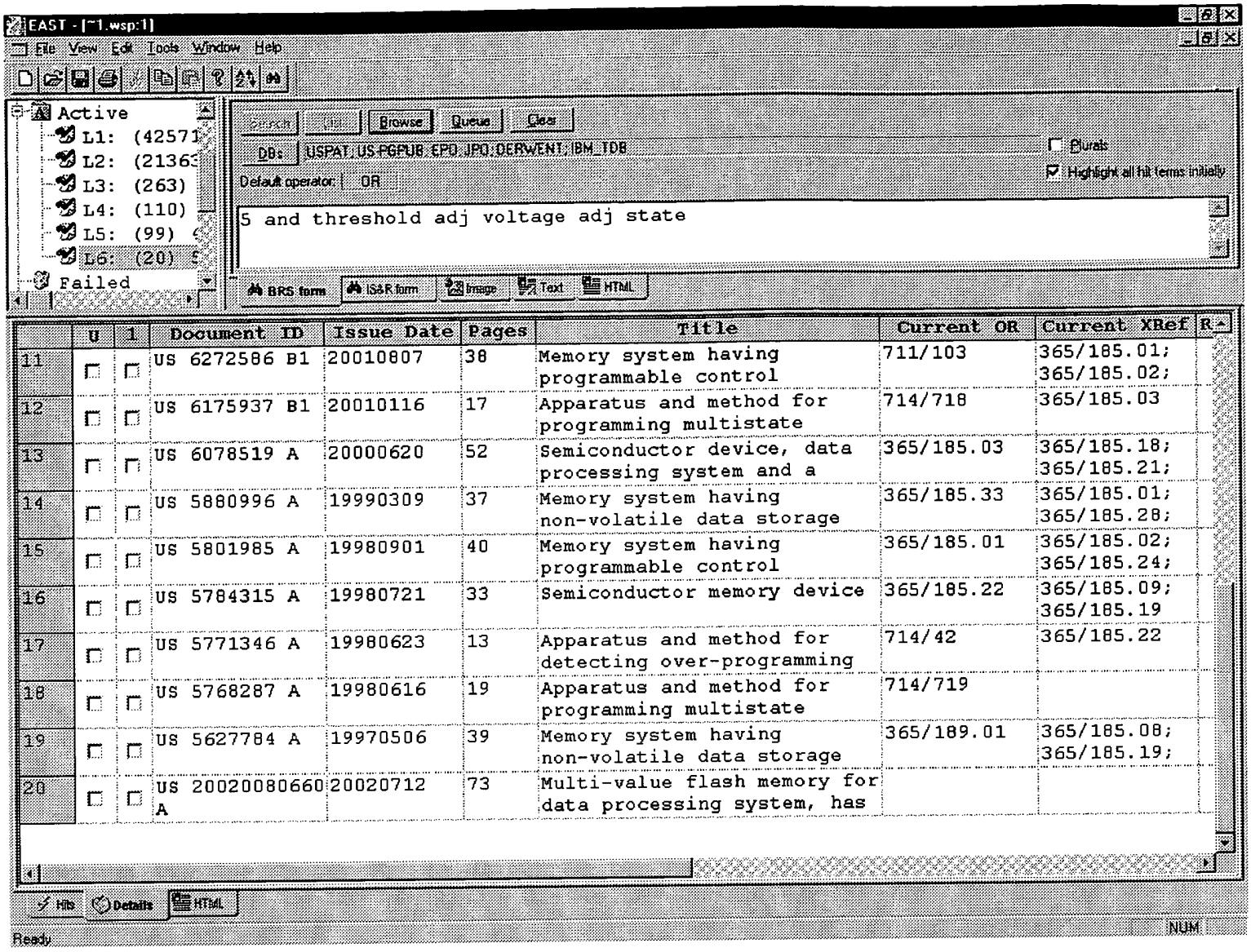


	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 20020144053 A1	20021003	43	Microcomputer, programming method and erasing method	711/103	711/154	
2	☐	☐	US 20020144052 A1	20021003	42	Microcomputer	711/103		
3	☐	☐	US 20020144035 A1	20021003	43	Microcomputer and data processing device	710/100		
4	☐	☐	US 20020080660 A1	20020627	73	Semiconductor device and data processing system	365/200		
5	☐	☐	US 20020032891 A1	20020314	51	Data processing system and data processing method	714/766		
6	☐	☐	US 20020027233 A1	20020307	42	Semiconductor device, microcomputer and flash	257/200		
7	☐	☐	US 20020008991 A1	20020124	53	Semiconductor device, data processing system and a	365/185.03		
8	☐	☐	US 6490195 B2	20021203	51	Semiconductor device, data processing system and a	365/185.03	365/185.18; 365/185.22	
9	☐	☐	US 6477090 B2	20021105	41	Semiconductor device, microcomputer and flash	365/189.09	365/185.21; 365/185.23;	
10	☐	☐	US 6301150 B1	20011009	51	Semiconductor device, data processing system and a	365/185.03	365/185.18; 365/185.21;	
11	☐	☐	US 6272586 B1	20010807	38	Memory system having programmable control	711/103	365/185.01; 365/185.02;	



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
11	☐	☐	US 6272586 B1	20010807	38	Memory system having programmable control	711/103	365/185.01; 365/185.02;	
12	☐	☐	US 6175937 B1	20010116	17	Apparatus and method for programming multistate	714/718	365/185.03	
13	☐	☐	US 6078519 A	20000620	52	Semiconductor device, data processing system and a	365/185.03	365/185.18; 365/185.21;	
14	☐	☐	US 5880996 A	19990309	37	Memory system having non-volatile data storage	365/185.33	365/185.01; 365/185.28;	
15	☐	☐	US 5801985 A	19980901	40	Memory system having programmable control	365/185.01	365/185.02; 365/185.24;	
16	☐	☐	US 5784315 A	19980721	33	Semiconductor memory device	365/185.22	365/185.09; 365/185.19	
17	☐	☐	US 5771346 A	19980623	13	Apparatus and method for detecting over-programming	714/42	365/185.22	
18	☐	☐	US 5768287 A	19980616	19	Apparatus and method for programming multistate	714/719		
19	☐	☐	US 5627784 A	19970506	39	Memory system having non-volatile data storage	365/189.01	365/185.08; 365/185.19;	
20	☐	☐	US 20020080660 A	20020712	73	Multi-value flash memory for data processing system, has			